L10

Quectel GPS Engine

Hardware Design Application Notes

L10_HD_AN01_V1.00

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Contents

Table Index

Figure Index

0. Revision history

Revision	Date	Author	Description of change
1.00	2009-08-05	Yong AN/Samuel HONG	Initial

1. Introduction

This document gives design recommendations Quectel's L10 module in the applications such as tracking and tracing, navigation. It includes design notes, reference circuits, PCB layout guides, and etc.

Table 1: Reference

SN	Document name	Remark
[1]	L10_HD	Hardware design document of L10 module
[2]	L10_EVB _UGD	L10 EVB User Guide

2. Product Concept

The L10 GPS module brings the high performance of the MTK positioning engine to the industrial standard. The module supports 210 PRN channels. With 66 search channels and 22 simultaneous tracking channels, it acquires and tracks satellites in the shortest time even at indoor signal level. This versatile, stand-alone receiver combines an extensive array of features with flexible connectivity options. The embedded FLASH memory provides capacity for storing user-specific configuration settings and allows for future update. L10 advanced jamming suppression mechanism and innovative RF architecture provide a high level of immunity for jamming, ensuring maximum GPS performance. The module supports location, navigation and industrial applications including autonomous GPS C/A, SBAS (including WAAS, EGNOS, MSAS), DGPS (RTCM), and AGPS.

The L10 is an SMD type module with the compact 22.4mm x 17.0mm x 3.0 mm form factor, which can be embedded in customer applications through the 28-pin pads. It provides all hardware interfaces between the module and customer's board.

- The UART port can help to develop customer's application easily.
- The USB port is available for faster data transmission and more flexibility
- The antenna interface supports passive and active antenna.

In order to obtain good performance with a GPS receiver module, there are a number of points that require careful attention during the design-in.

- Power supply
  Good performance requires a clean and stable power supply.
- Interfaces
  Ensure correct connection, rate and message setup on the module and your host system.
- Antenna interface
  For optimal performance seek short routing, matched impedance and no stubs.

The module is fully RoHS compliant to EU regulation.

3. Power

3.1. Power Management

3.1.1 VCC

The main power supply is fed through the **VCC** pin. It is important that the system power supply circuitry is able to support the peak power. In order to define a battery capacity for specific applications the sustained power figure should be used. It is suggested that the power supply must be capable of providing sufficient current up to 150mA.

The circuit design of the power supply depends strongly on the power source where this power is drained. Good performance requires a clean and stable power supply with minimal ripple. Care needs to be exercised in selecting a strategy to achieve this. Series resistance in the **VCC** supply line can negatively impact performance. For better performance, use an LDO to provide a clean supply at **VCC** and consider the following:

- Wide power lines or even power planes are preferred.
- Place LDO and a filter at **VCC** near the module.
- Avoid resistive components in the power line (e.g. narrow power lines, coils, resistors, etc.).

An LDO (Low Dropout Regulator) device, such as Torex (http://www.torex.co.jp/english) XC6219B332MR is recommended. Typical output voltage value is 3.3V. The reference design circuit is shown in Figure 1.

3.1.2 VDDUSB

VDDUSB supplies for the I/Os of the USB interface. When the USB port is not used, the **VDDUSB** pin must be connected to **GND**. Otherwise, **VDDUSB** must be connected to an external LDO so as to comply with USB specifications. Typical output voltage of the LDO is 3.3V. The reference circuit is shown in Figure 1.

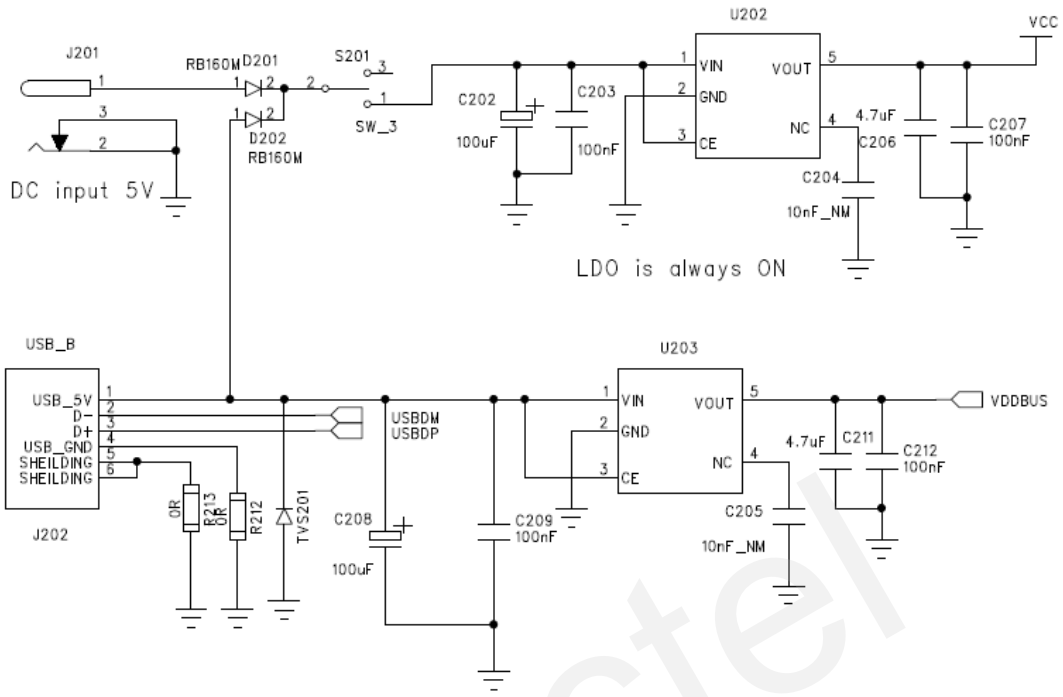


Figure 1: Power supply reference circuit

In Figure 1, **VCC** is supplied by both the DC input and the 5V input of the USB connector which is optional according to customer's requirement. LDO (power supply IC U202) could be always on, but it can be controlled by host MCU through the CE pin of LDO to shut off the output voltage so as to save power, as shown in Figure 2.

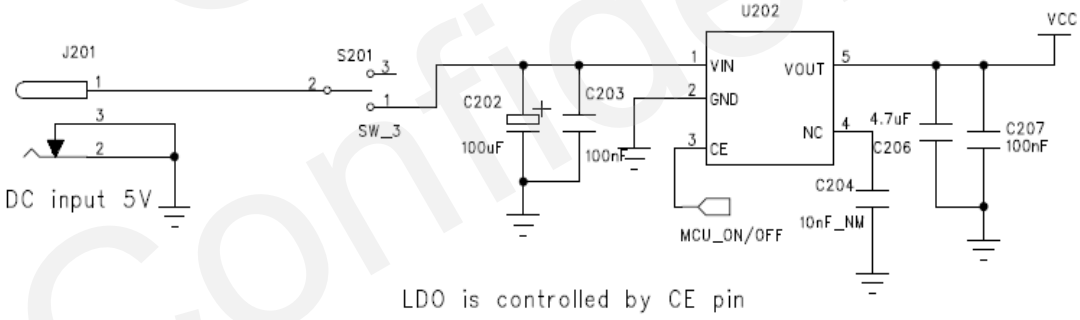


Figure 2: Power supply reference circuit controlled by MCU

3.1.3 V_BCKP

In case of a power failure on pin **VCC**, the real-time clock and backup RAM are supplied through pin **V_BCKP**. This enables the L10 module receiver to recover from a power failure with either Hot Start or Warm Start (depending on the duration of VCC outage) and to maintain the configuration settings. If no backup battery is connected, the receiver performs Cold Start at power up.

When **V_BCKP** is lower than **VCC**, **V_BCKP** will not be drained by the internal RTC LDO as shown in Figure 3. Thus, **V_BCKP** is recommended to be lower than **VCC**.

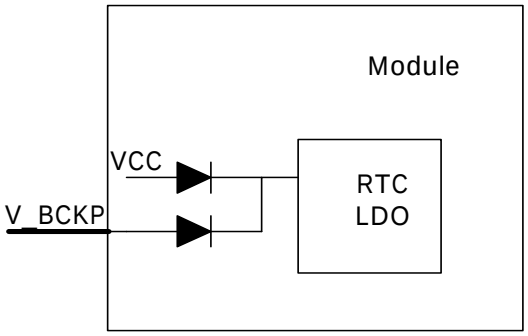


Figure 3: V_BCKP internal block diagram of module

The **V_BCKP** pin does not implement charging for rechargeable battery which is used in customer's design. It is necessary to add a charging circuit for rechargeable battery, as shown in Figure 4.

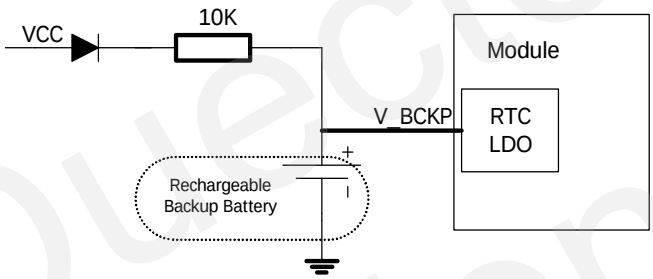


Figure 4: Reference charging circuit for rechargeable battery

Note: In order to achieve a minimal reacquisition time, connect a backup battery to V_BCKP.

3.2. V_ANT

The L10 module supports power supply and supervision for active antenna. There are two ways to supply power for active antenna through **V_ANT** pin. The first method is to connect the **VCC_RF** pin to the **V_ANT** pin if the **VCC_RF** voltage is suitable for powering the active antenna. The second method is to apply an external LDO and connect its output to the **V_ANT** pin if the **VCC_RF** voltage isn't fit for powering the active antenna.

3.3. Power Save

There are two ways to minimize the power consumption. The first one is to shut off the power supply to module by controlling CE pin of VCC LDO, as indicated in Figure 2. The other is to drive module into Standby Mode by changing pin **EXINT0** from high to low and holding at low level. For more details, please refer to document [1].

4. Digital I/O Connection

If the voltage level of peripheral interface circuit does not match to module's interface, the power consumption of the system could increase, and could even cause the module damaged.

- Each digital I/O of the module operates in a 2.8V logic level inside the module. The voltage level of those digital interfaces connected to the module should match to the electrical characteristics of the module listed in Table 2. Otherwise, a level shifter circuit must be inserted between the host and the module.

Table 2: Digital I/O electrical characteristics

SYMBOL	MIN	MAX	UNITS
V_{IL}	-0.3	0.8	V
V_{IH}	2.0	3.6	V
V_{OL}	-0.3	0.4	V
V_{OH}	2.4	3.1	V

- For direct connection between I/Os, please pay attention to I/Os' input or output configuration. If the I/O direction configuration conflicts with each other, the power consumption could increase, and the module could be very hot, and even be damaged. For example, it is forbidden that user's I/O outputs a low level while module's connected I/O outputs a high level.

4.1 EXTINT0

The **EXTINT0** pin is an external interrupt input pin and an edge trigger interrupt. This pin is pulled up internally in module, and it holds a high level after module is powered on. When the **EXTINT0** pin is changed from high to low and is held low level, the module will enter Standby Mode. When the **EXTINT0** pin is changed from low to high and is held high level, the module will exit from Standby Mode.

4.2 AOK

AOK can output antenna status message. It outputs a low level when the active GPS antenna is assembled and operating normally. When the GPS antenna is not assembled or short-circuited, it outputs a high level to alarm host controller.

4.3 RESET_N

L10 module can be reset by driving **RESET_N** to low level for a certain time and then release it. An open drain driver circuit is suggested in application to control **RESET_N**. For more details, please

refer to document [1].

5. Serial Interface

UART port (**TXD1**/**RXD1**) is the default serial interface. It supports data baud-rate from 4800bps to 115200bps. The default setting is 9600bps, 8 bits, no parity bit, 1 stop bit, no hardware flow control. It is used to connected to host MCU or DTE (Data Terminal Equipment). When design-in, level match must be considered each other. The DC characteristics of UART port are listed in Table 3 and must be complied.

Table 3: UART electrical characteristics

SYMBOL	MIN	MAX	UNITS
V_{IL}	-0.3	0.8	V
V_{IH}	2.0	3.6	V
V_{OL}	-0.3	0.4	V
V_{OH}	2.4	2.9	V

If the voltage level of UART pins in DTE and the module doesn't match with each other, level shifter circuit should be inserted. The following cases are recommended.

5.1. Communicate with DTE

It is recommended to design the level shift circuit by choosing open drain output buffer (e.g. NC7WZ07) or discrete transistor.

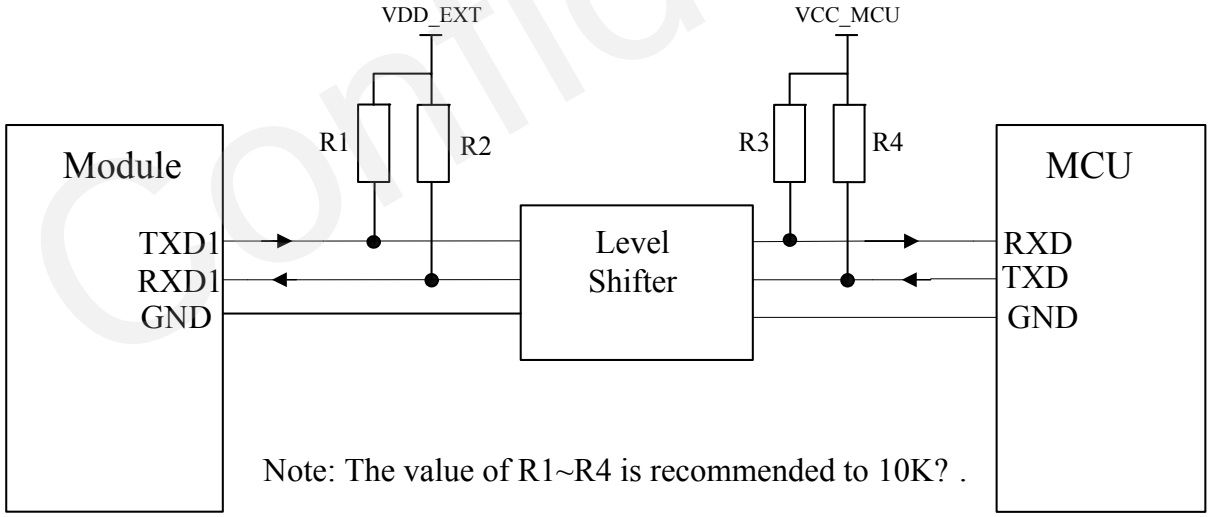


Figure 5: The reference level shifter by using open drain output buffer

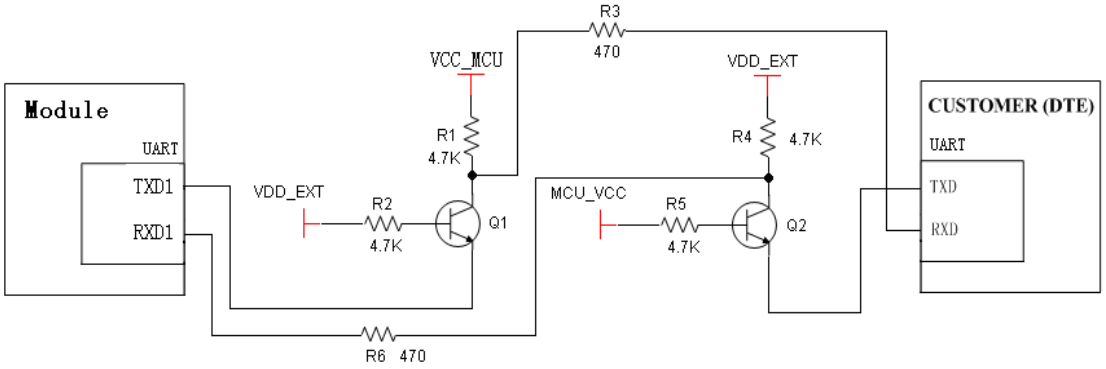


Figure 6: The reference level shifter by using bipolar transistor

Note:VDD_EXT should be 2.8V for the module interface. VCC_MCU is the voltage for host MCU interface.

5.2. Communicate with the RS-232 Port of PC

Table 4: RS-232 electrical characteristics

Logic level	Transmitter capable	Receiver capable	Unit
Logic 0	+5~+15	+3~+25	V
Logic 1	-5~-15	-3~-25	V
Undefined		-3~+3	V

It is suggested to design the level shifter by using RS-232 transceivers, e.g. SP3230.

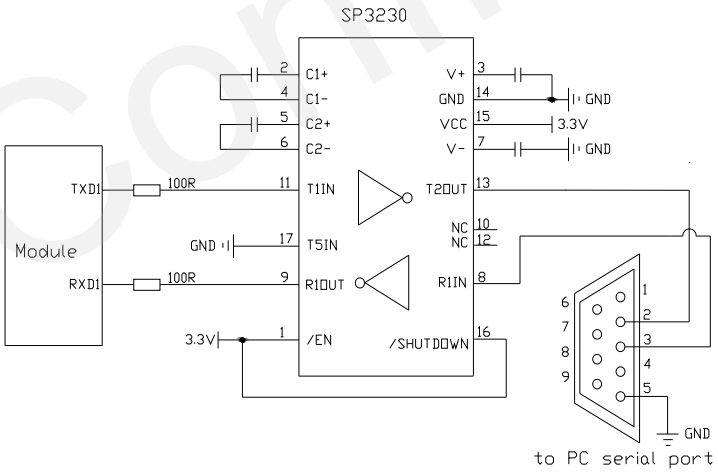


Figure 7: RS-232 level shift circuit

6. USB Interface

The USB (Universal Serial Bus) port can be used for GPS command and data transfer, and firmware upgrade. It is USB 2.0 Full Speed compatible.

7. Reference Design

For a typical design with L10 the following functions and pins should be considered:

- Connect the power supply to **VCC**.
- **VDDUSB** must be connected to an external LDO of 3.3V so as to comply with USB specifications, otherwise connect to GND if the USB port is not used.
- Assure an optimal ground connection to all ground pins of the module.
- Connect antenna to **RF_IN** through a 50Ω transmission line and choose right power supply for active antenna by internal or external power source.
- If Hot Start and Warm Start are required, connect a backup battery to V_BCKP.
- Consider the necessity of using **TIMEPULSE**, **EXINT0**, **RESET_N** and **AOK** pins.

The L10 module supports both passive and active antenna. The recommended specification of antenna is listed in Table 5.

Table 5: Antenna specification for L10 module

Antenna type	Specification
Passive antenna	Center frequency: 1575.42 MHz Bandwidth: >20 MHz Gain: >0 dBi Polarization: RHCP
Active antenna	Center frequency: 1575.42 MHz Bandwidth: >5 MHz Minimum gain: 15-20dB(compensate signal loss in RF cable) Maximum noise figure: 1.5dB Maximum gain: 50dB Polarization: RHCP

7.1 Passive Antenna Design

Passive antenna doesn't require a DC bias voltage and can be connected to **RF_IN** pin directly. **V_ANT** should be connected to GND. It is always beneficial to reserve a passive matching network between the antenna and the **RF_IN** port of the module. A DC-blocking capacitor is needed between the **RF_IN** pin and the matching circuit. For more details about matching network design please refer to Chapter 8.3.

Figure 8 is the reference design for passive antenna using USB port and Figure 9 is the reference design for passive antenna without using USB port.

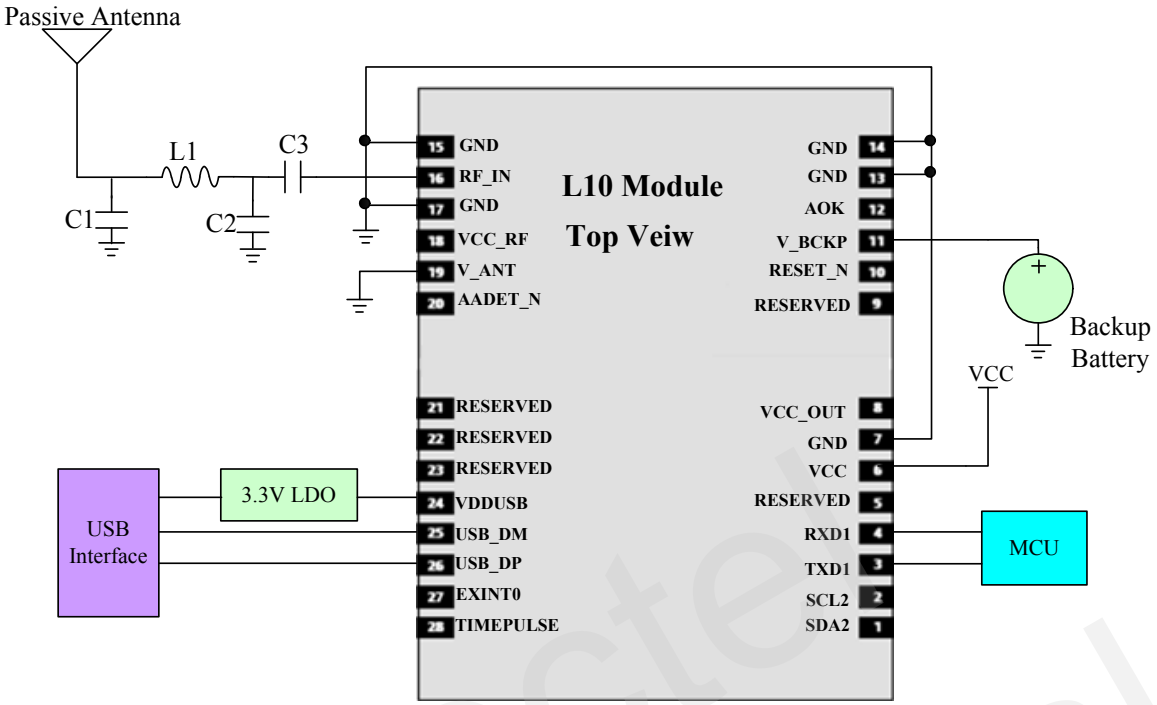


Figure 8: Passive antenna design using USB port

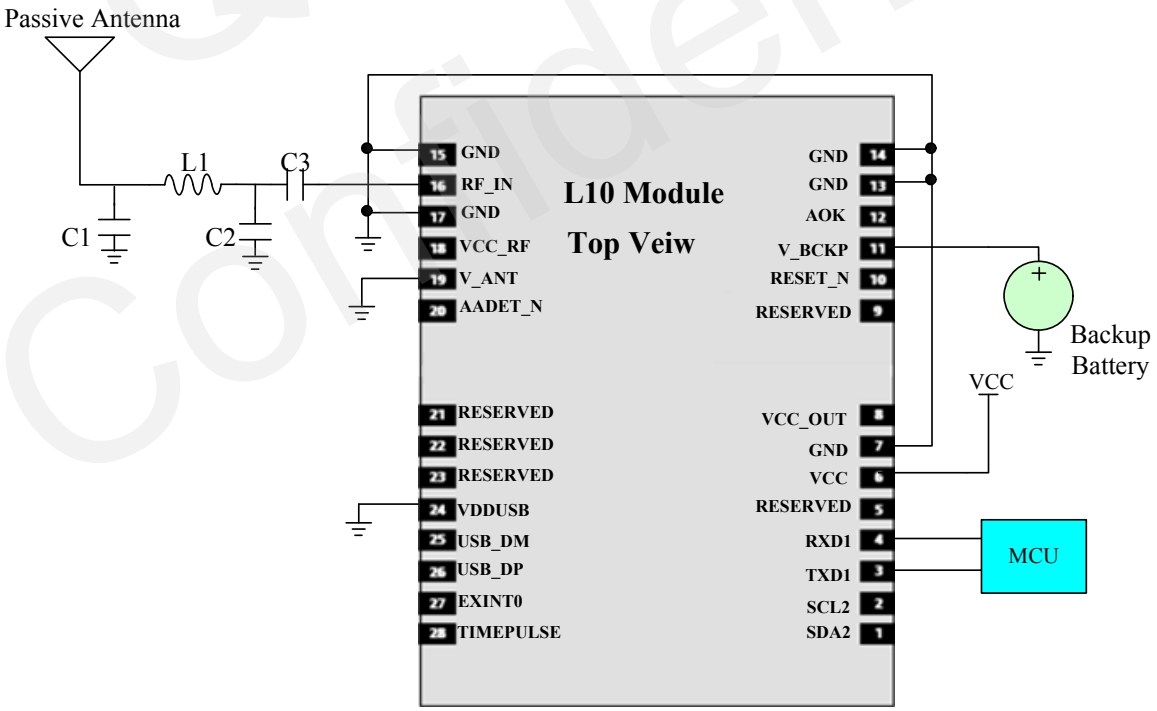


Figure 9: Passive antenna design without using USB port

7.2 Active Antenna Design

Active antenna has an integrated low-noise amplifier which can be connected to RF_IN directly. When an active antenna is connected to **RF_IN**, the integrated low-noise amplifier within the antenna needs to be powered by correct voltage through pin **V_ANT**. Usually, the supply voltage is fed to the active antenna through a coaxial RF cable. A common active antenna consumes current between 5mA and 20mA. The 27nH inductor inside the module can separate the RF signal from the **V_ANT** pin and routes the bias supply to the active antenna.

The block diagram of power supply part for active antenna is shown in Figure 10.

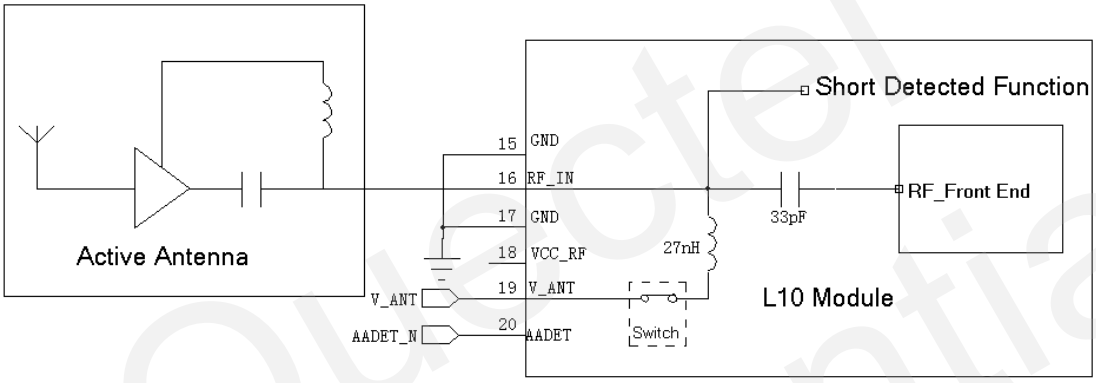


Figure 10: Active antenna biasing

If **VCC_RF** is able to power the active antenna, **VCC_RF** could be connected directly to **V_ANT**. A reference circuit is shown in Figure 11.

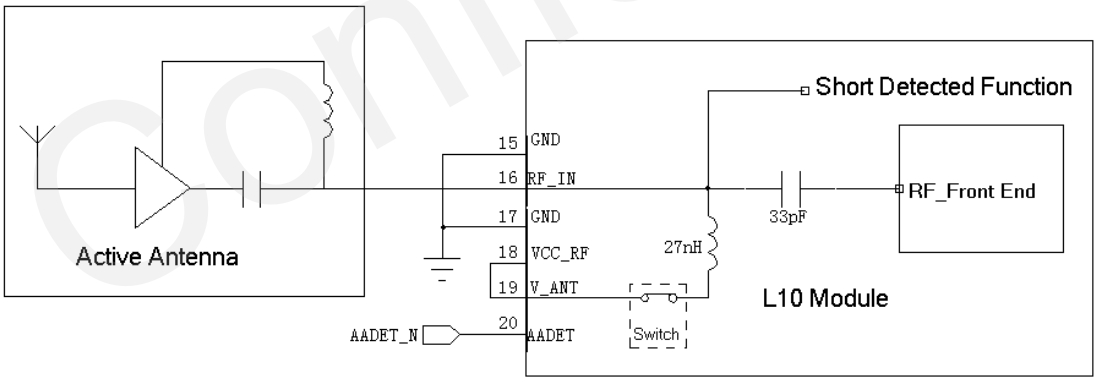


Figure 11: Active antenna with VCC_RF

If **VCC_RF** output can't meet the requirement for powering the active antenna, an external LDO could be used. The output of the external LDO can be connected to **V_ANT**. A reference circuit is shown in Figure 12.

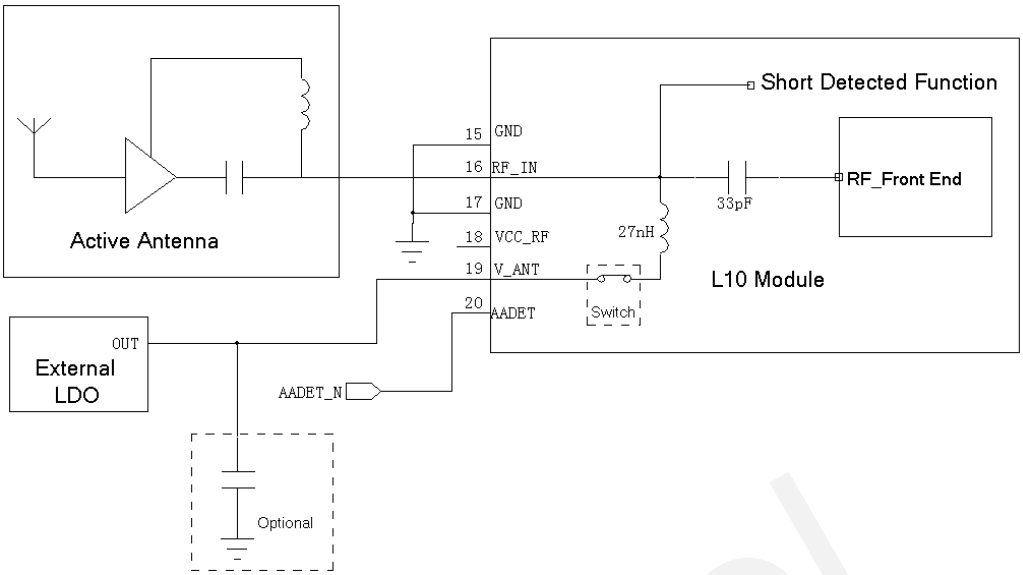


Figure 12: Active antenna with external LDO

If an external power supply and an external inductor are used to power the active antenna, the short-circuit detection function could still work, but it couldn't cut off the external power supply. So this way is not recommended.

7.3 Open-circuit Supervision for Active Antenna

AADET is used for open-circuit detection. Open-circuit detection can be supported with an additional external circuit. The reference design of the external circuit is shown in Figure 13.

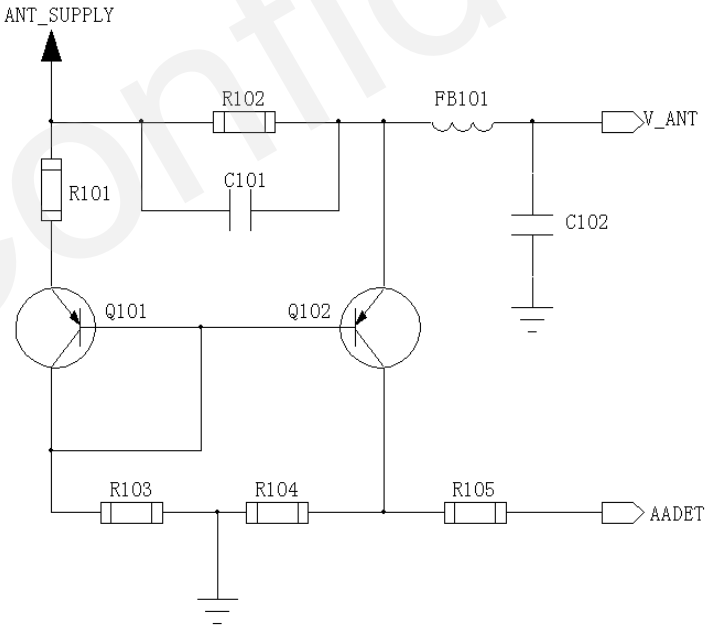


Figure 13: External detection circuit for open-circuit of active antenna

The BOM of the components in Figure 13 is listed in Table 6.

Table 6: List of BOM

Reference	Part number	Description	Remark
R101	RC0402JR-0715RL	15R +/-5% 1/16W 0402	YAGEO
R102	RC0805FR-0710RL	10R +/-5% 1/4W 0805	YAGEO
R103 R104 R105	RC0402JR-0710KL	10K +/-5% 1/16W 0402	YAGEO
C101	GRM188R60J475KE19D	4.7uF +/-10% X5R 6.3V 0603	MURATA
C102	C1005X5R1A104KT	100nF +/-10 X5R 10V 0402	TDK
Q101 Q102	2SA1037AKT146	PNP SOT23 Transistor	ROHM
FB101	BLM15BD102SN1	Bead（0402）1000ohm	MURATA

The electrical characteristics of pin AADET is listed in Table 7.

Table 7: AADET electrical characteristics

SYMBOL	MIN	MAX	UNITS
V_{IL}	-0.3	0.5	V
V_{IH}	2.0	5.5	V

7.4 Short-circuit Supervision for Active Antenna

If the active antenna is short-circuited, the module would turn off the power supply to the antenna immediately. When the short-circuit problem is removed, it will recover the power supply to the active antenna.

7.5 Active Antenna Status Report

The status of the active antenna is reported in a NMEA message (defined as $GPTXT) at start-up and on every change.

Table8: Active antenna status report

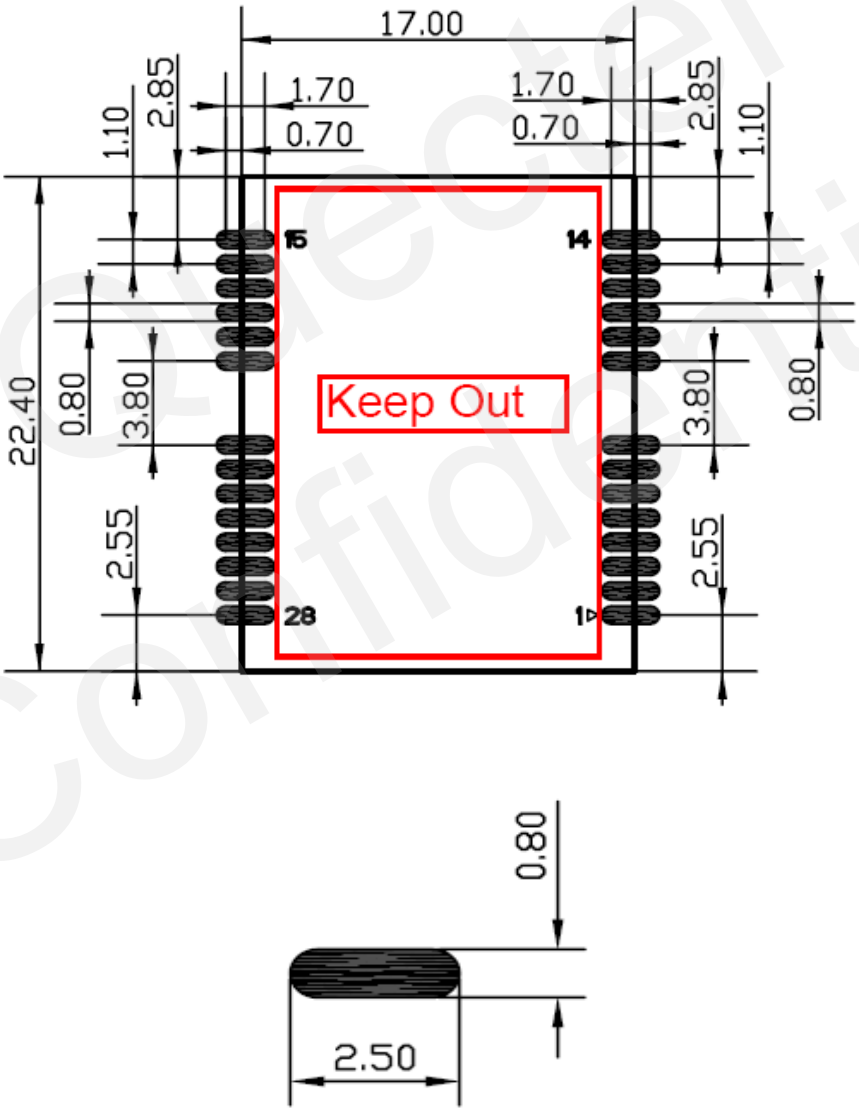
Status	Report message
Status=OK	$GPTXT,01,01,02,ANTSTATUS=OK*3B
Status=OPEN	$GPTXT,01,01,02,ANTSTATUS=OPEN*2B
Status=SHORT	$GPTXT,01,01,02,ANTSTATUS=SHORT*6D

If external open-circuit detection circuit is not applied, the open-circuit detection function wouldn't work. In this case, the reported antenna status is always OK when the antenna is OK or Open. Nonetheless, the short-circuit detection circuit inside the module will still work and report the short-circuit status normally.

8. Layout Design Guide

This section provides important information for designing a reliable and sensitive GPS system. GPS signals at the surface of the Earth are about 15dB below the thermal noise floor. Signal loss at the antenna and the RF connection must be minimized. When defining a GPS receiver layout, the placement of the antenna with respect to the receiver, as well as grounding, shielding and jamming from other digital devices are crucial issues and need to be considered very carefully.

8.1 Footprint of Recommendation



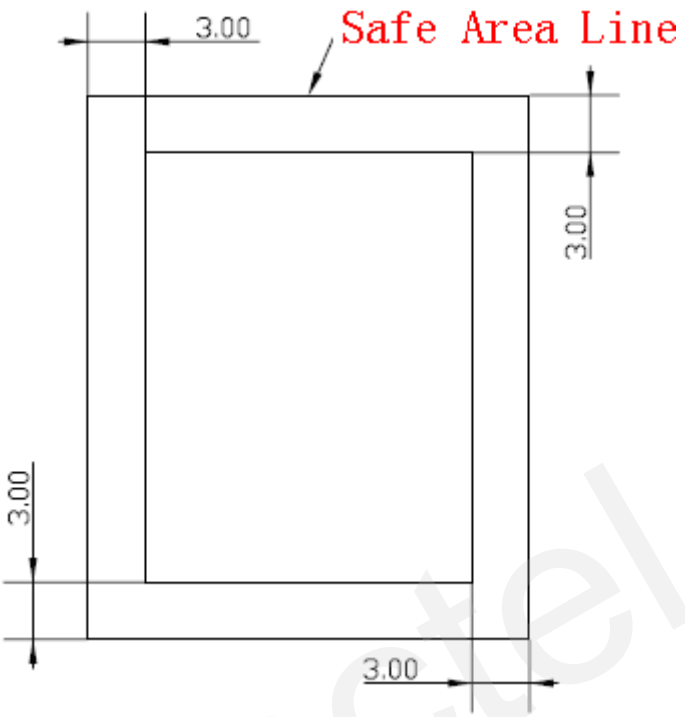


Figure 14: Footprint of recommendation（Unit: mm）

Note 1：Keep out on the host board below the module and the keep-out area should be covered by solder mask and top silk layer for isolation between the top layer of host board and the bottom layer of the module.
Note 2：For easy maintenance of this module and accessing to these pads, please keep a distance no less than 3mm between the module and other components in host board.

8.2 Placement

A very important factor in achieving maximum GPS performance is the placement of the receiver in host PCB. The connection to the antenna must be as short as possible to avoid jamming into the very sensitive RF section. Make sure the RF circuits are clearly separated from any other digital circuits on host board. To achieve this, position the receiver digital part towards your digital section of the host PCB. Care must also be exercised with placing the receiver in proximity to circuitry that can emit heat. The RF part of the receiver is very sensitive to temperature and sudden changes can have an adverse impact on performance.

Note: The RF part of the receiver is a temperature sensitive component. Avoid high temperature drift and air vents near the receiver.

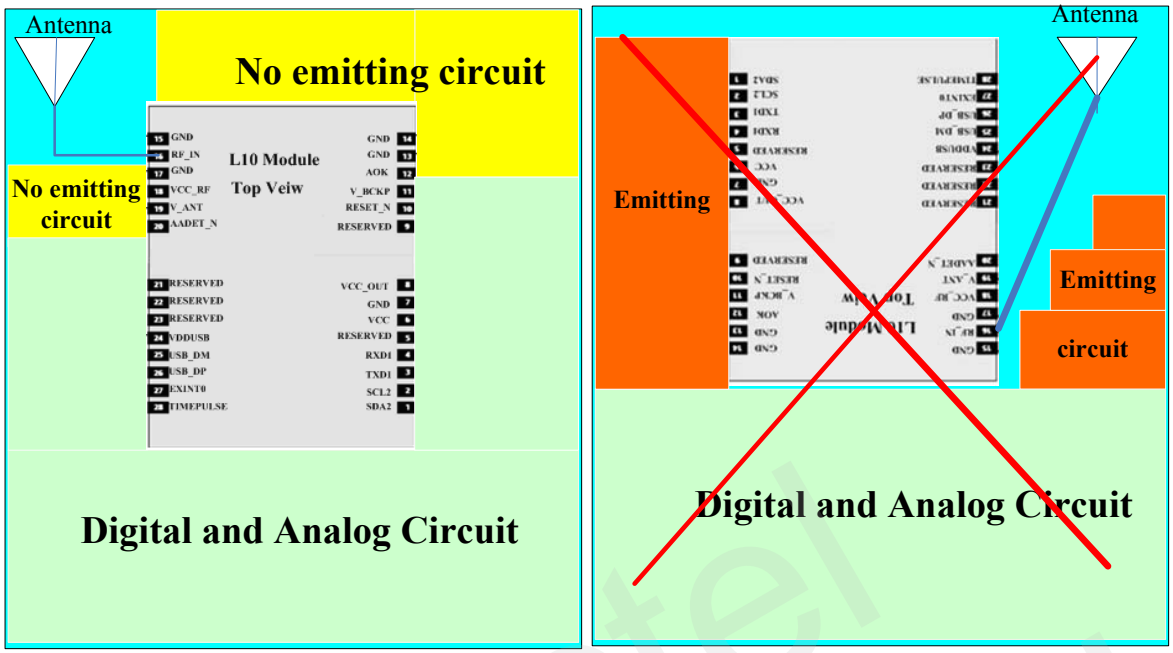


Figure 15: Placement compare

8.3 Recommended Impedance Matching Circuit

The impedance of L10's **RF_IN** port is 50Ω.The impedance of active antenna is always close to 50Ω, so the antenna can be connected to the **RF_IN** port directly. But the impedance of passive antenna may be not close to 50Ω. In this case, a T-type or π-type matching circuit should be inserted between RF transmission line and antenna. The matching components should be placed as close as possible to the antenna connector.

Figure 16 and Figure 17 show the reference designs of T-type and π-type matching circuits.

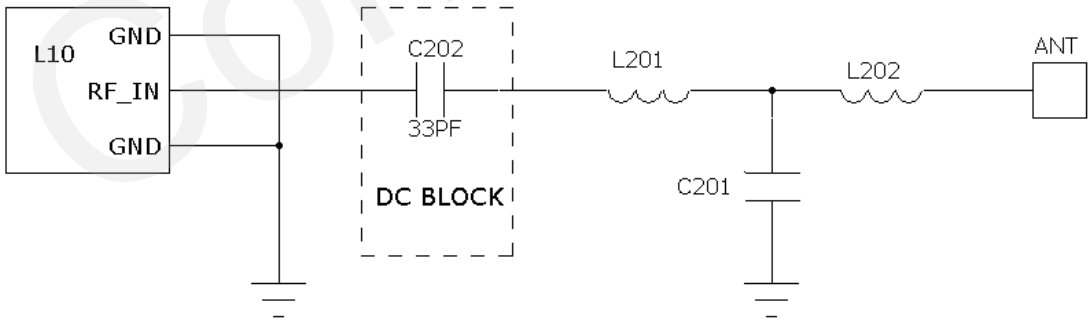


Figure 16: T-type matching circuit

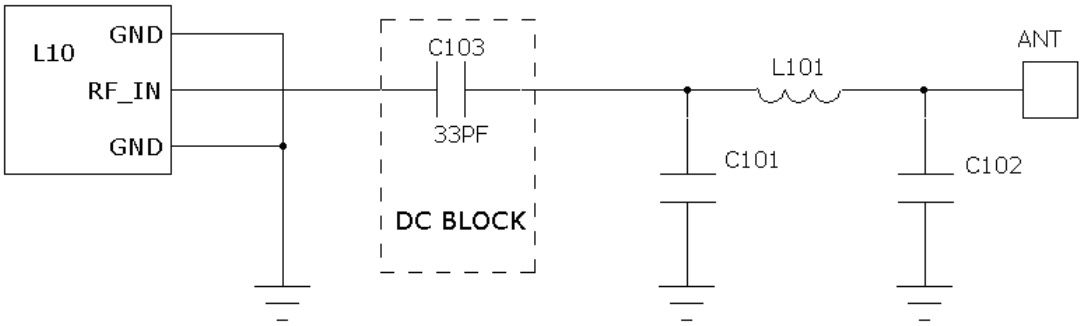


Figure17: π-type matching circuit

Note: The impedance of traces in bold must be 50Ω.

8.4 Matched RF Transmission Line Design

In PCB layout, a matched RF transmission line has fixed characteristic impedance, which is called Z_0, from its source to its load. The source should have an internal resistance of Z_0 and the resistance of matching load should close to Z_0.

Since the impedance of L10's **RF_IN** port is 50Ω, the impedance of the RF transmission line from this port to the antenna or the matching circuit should also be made to 50Ω.

More than twelve different types of transmission line can be created on a PCB simply by controlling trace geometry, and some of them are shown in Figure 18.

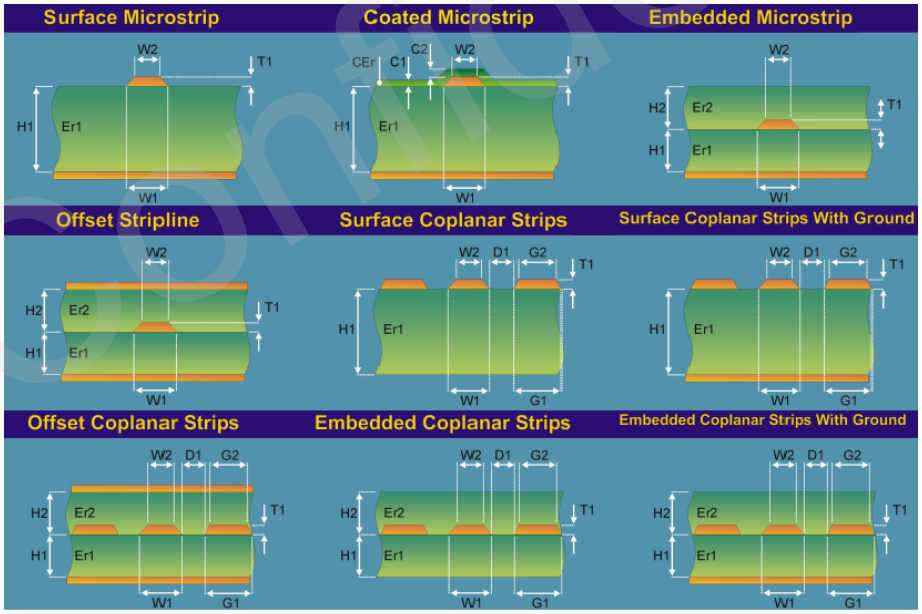


Figure 18: L10 RF_IN PCB layout

Customer may adopt one or certain types of them to design RF trace. Upon the demand of application design, the number of PCB layer can be different such as two and four. Each type of

PCB has corresponding “stack-up”. The “stack-up” is the name given to the order of the various etched copper foil and dielectric layers that are laminated together under pressure and heat to make a PCB.

Customer can calculate 50Ω RF trace width by EDA tools such as CITS or APPCAD, or send the “stack-up” to Quectel, and we can help to calculate it.

8.5 PCB Layout Consideration

PCB Layout is essential to the performance of customer’s product. Here are some rules that should be followed:

- Impedance control
  Control the impedance of RF trace as close as possible to 50Ω. If the thickness between **RF_IN** pad and the ground layer is less than 0.3mm, it could significantly decrease the output power. Therefore, when they are too close, we strongly suggest removing the copper in the layer beneath the **RF_IN** pad. If RF trace routes to another layer, add GND via along with it to keep GND integral. The clearance between RF trace and ground plane in same layer should be at least twice the RF trace width.
- Make RF trace as short as possible
  Place the module and the matching circuit near the antenna interface. Shorten the length of RF trace. Long RF trace proportionally increases the loss of RF signal, and adversely affect the value of CNR, especially while passive antenna is adopted.
- Protect RF trace
  Avoid placing noise generating traces such as digital signal or clock line near RF trace in the same layer. Carefully route other traces in the layers adjacent to the RF trace, remember not to route in parallel with the RF trace. If possible, keep those traces far away from the RF trace.

9. ESD

Electrostatic discharge (ESD) is the sudden and momentary electric current that flows between two objects at different electrical potentials caused by direct contact or induced by an electrostatic field. Without cautious handling, it may cause damage to the GPS receiver.

All pins in L10 can stand ESD Air Discharge of ±8KV.

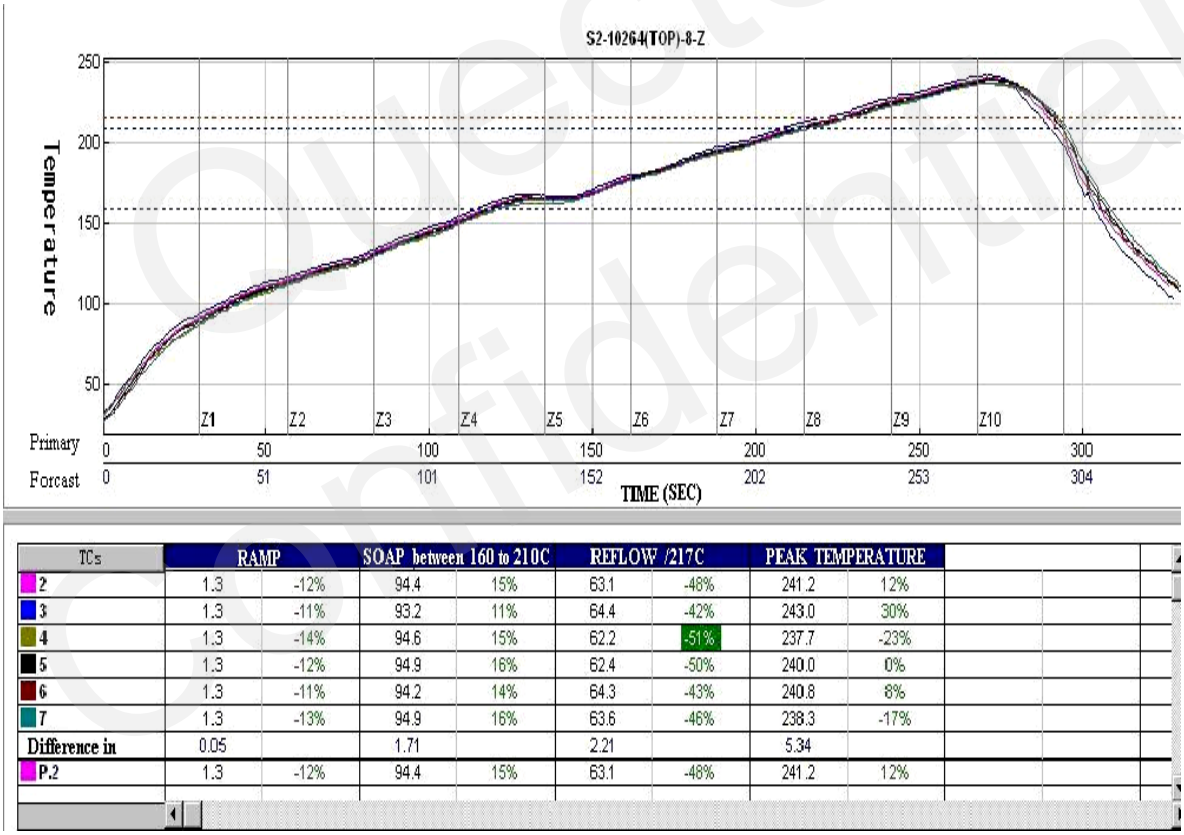
10. Recommended SMT Processing

10.1. Basic Configuration

Table 9: Recommended requirements

Item	Data
Stencil Thickness	150um~180um
Soldering Paste Print Press	1.4*0.01mpa

10.2. Reflow Soldering Profile



TCs	RAMP		SOAP between 160 to 210C		REFLOW /217C		PEAK TEMPERATURE	
2	1.3	-12%	94.4	15%	63.1	-48%	241.2	12%
3	1.3	-11%	93.2	11%	64.4	-42%	243.0	30%
4	1.3	-14%	94.6	15%	62.2	-51%	237.7	-23%
5	1.3	-12%	94.9	16%	62.4	-50%	240.0	0%
6	1.3	-11%	94.2	14%	64.3	-43%	240.8	8%
7	1.3	-13%	94.9	16%	63.6	-46%	238.3	-17%
Difference in	0.05		1.71		2.21		5.34	
P.2	1.3	-12%	94.4	15%	63.1	-48%	241.2	12%

Figure 19: The recommended ramp-soak-spike reflow profile

10.3. Optical Inspection

After soldering the L10 module, implementing an optical inspection would be helpful to check whether:

- The module is properly aligned and centered over the pads.

- All pads are properly soldered.
- No excess solder has created contacts to neighbouring pads, or possibly to pad stacks and via nearby.

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